E0C88F360

8-bit Single Chip Microcomputer

Preliminary

Low Voltage Operation Products

- Evaluation Chip with Flash Built-in
- Compatible with E0C88861/862/832/348/317/316/308
- On-board Writing Supported

■ DESCRIPTION

The E0C88F360 is a CMOS 8-bit microcomputer composed of the core CPU E0C88 (MODEL3), rewritable ROM (Flash), RAM, dot-matrix type LCD driver, three types of timers and asynchronous/clock synchronous selectable serial interface. The E0C88F360 has a built-in large-capacity Flash ROM (60K × 8 bits) and a RAM (2K × 8 bits), and is upper compatible with the E0C88861, E0C88862, E0C88832, E0C88348, E0C88317, E0C88316 and E0C88308. The E0C88F360 can be used as a MTP (Multi-Time Programming) when developing programs.

■ FEATURES

- Core CPU .... E0C88 (MODEL3) CMOS 8-bit core CPU
- OSC1 oscillation circuit .... 32.768kHz (Typ.) crystal oscillation circuit
- OSC3 oscillation circuit .... 8.2MHz (Max.) crystal/ceramic oscillation circuit
- Instruction set .... 608 types (usable for multiplication and division instructions)
- Instruction execution time .... 0.244 µsec/8.2MHz (for 2-clock instructions)
- PROM (Flash EEPROM) .... 61,440 × 8 bits
  Supports serial- and parallel-programming method using the exclusive ROM writer
- RAM .... 2K-byte RAM
  3,216-bit display memory
- Bus line .... Address bus : 19 bits (shared with output ports)
  Data bus : 8 bits (shared with I/O ports)
  $\overline{\text{CE}}$ signal : 4 bits (shared with output ports)
  $\overline{\text{WR}}$ signal : 1 bit (shared with output port)
  $\overline{\text{RD}}$ signal : 1 bit (shared with output port)
- Input port .... 10 bits (usable for $\overline{\text{EVIN}}$ and $\overline{\text{BREQ}}$ signal inputs)
- Output port .... 9 bits (usable for buzzer, LCD control, FOUT, TOUT and $\overline{\text{BACK}}$ signal outputs)
- I/O port .... 8 bits (usable for serial I/O and analog comparator inputs)
- Serial interface .... 1 ch. (8-bit clock synchronous or asynchronous system)
- Timer .... Programmable timer (8 bits) : 2 ch. (usable as a 1-ch. 16-bit timer)
  Clock timer (8 bits) : 1 ch.
  Stopwatch timer (8 bits) : 1 ch.
- LCD driver .... Dot-matrix type (supports 5 × 8 or 5 × 5 dot font)
  51 segments × 32 commons, 67 segments × 16 or 8 commons
  LCD power supply circuit built-in (boostor type, 5 potentials)
- Sound generator .... Envelope and volume control functions built-in
- Watchdog timer .... Built-in
- Analog comparator .... 2 ch.
- A/D converter .... 4 ch., 10-bit resolution, maximum error = ±3LSB
  (not available if analog comparator is used)

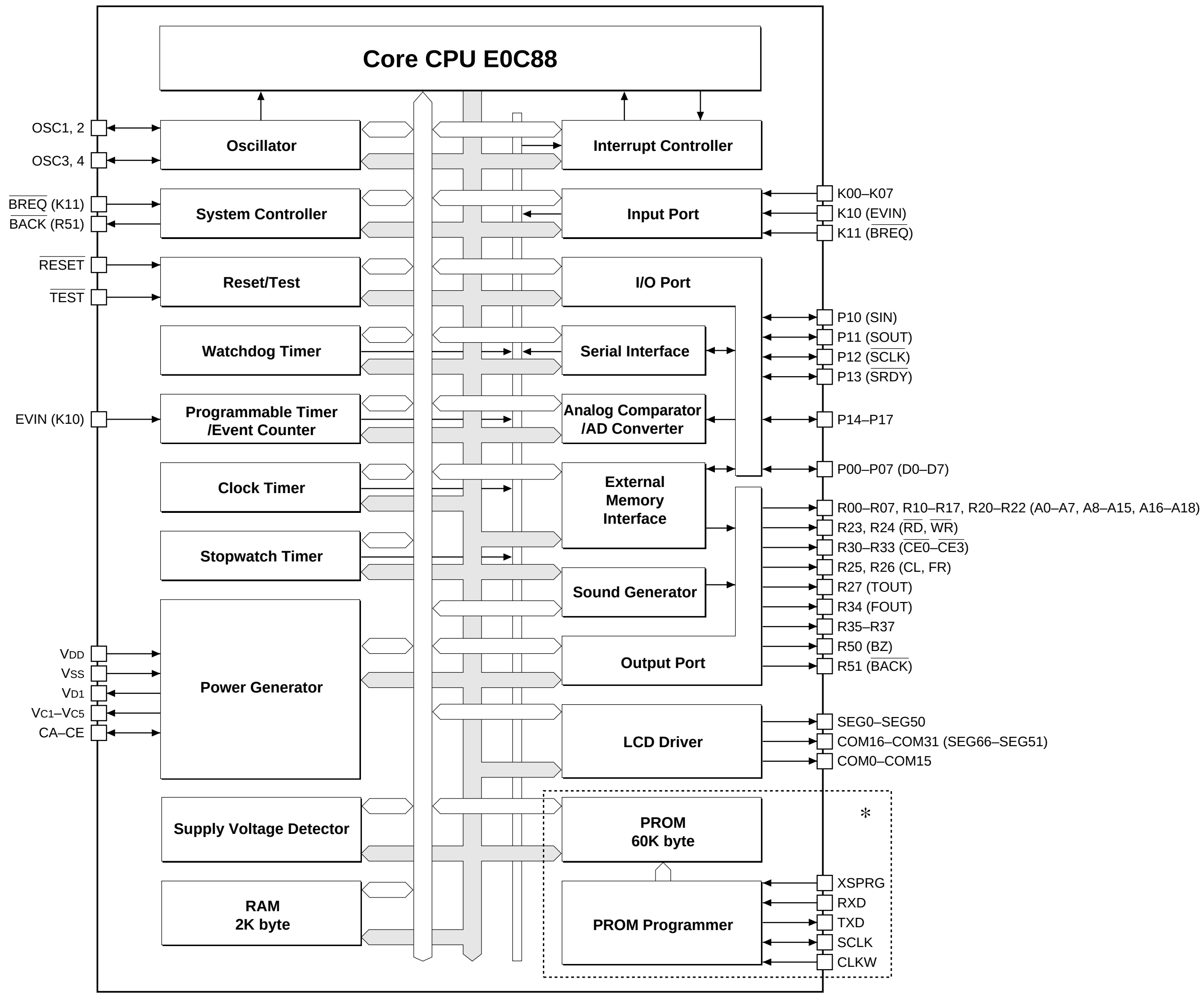
- Supply voltage detection (SVD) circuit ... 16-level detection
- External interrupt .... Input port interrupt : 2 systems (3 types)
- Internal interrupt .... Timer interrupt : 3 systems (9 types)
  Serial interface interrupt : 1 system (3 types)
  A/D converter interrupt : 1 system (1 type)
- Power supply voltage .... Normal mode : 2.4V to 5.5V (Max. 4.2MHz) V_{D1} = 2.2V
  Low-power mode : 1.8V* to 3.5V (Max. 50kHz) V_{D1} = 1.6V
  High-speed mode : 3.5V to 5.5V (Max. 8.2MHz*) V_{D1} = 3.3V
- Current consumption ....

	E0C88F360 *	E0C88862 (measured value)
HALT mode :	3µA (Typ., normal mode)	2µA (Typ., normal mode)
Run (32kHz) :	18µA (Typ., normal mode)	10µA (Typ., normal mode)
Run (4MHz) :	2mA (Typ., normal mode)	1.5mA (Typ., normal mode)

- Package .... QFP18-176pin (plastic) or chip

* Design objective

■ BLOCK DIAGRAM



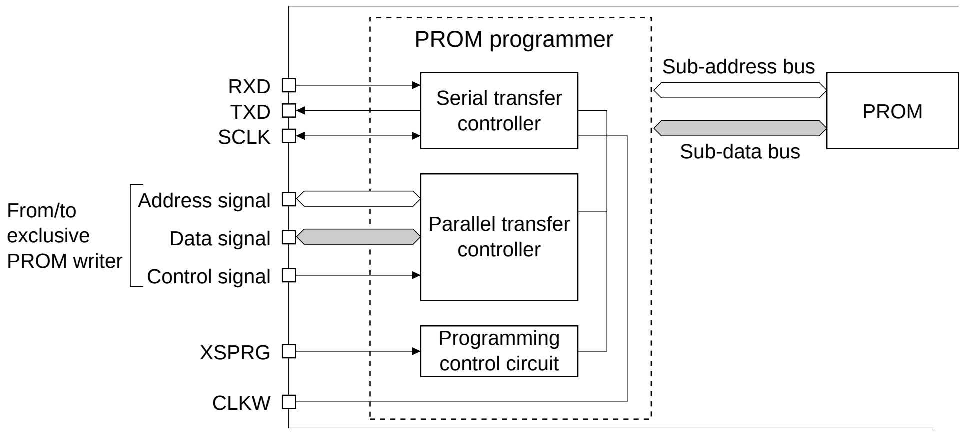
* The PROM block indicated with a dotted line differ from the E0C88xxx.

■ PROM PROGRAMMER AND OPERATING MODES

The biggest difference between the E0C88F360 and the E0C88xxx is that the E0C88F360 contains Flash EEPROM as the ROM that allows the user to write data to it using the exclusive ROM writer (UNIVERSAL ROM WRITER II). The E0C88F360 also has a built-in PROM programmer that controls writing data to the PROM.
The following explains the PROM programmer and the operating modes that are added for the programming operation.

● Configuration of PROM Programmer

The configuration of the PROM programmer is shown below.



The PROM programmer supports Serial Programming for writing data received in serial transfer and Parallel Programming that uses a parallel transfer. The programming method will be described later.

Terminals

The PROM programmer uses the following input/output terminals. The following sections will explain handling the terminals in each operating mode.

XSPRG: PROM serial programming mode setting terminal
RXD: Serial data receive terminal
TXD: Serial data transmit terminal
SCLK: Serial clock input/output terminal
CLKW: Serial programming source clock (3.072 MHz) input terminal

The parallel programming mode uses other terminals in addition to the terminals above. However, it is not necessary to switch the lines on the board, because the IC is programed by directly installing it to the exclusive PROM writer (UNIVERSAL ROM WRITER II).

● Operating Modes

Three operating modes are available in the E0C88F360: one is for normal operation and the others are for programming.

1) Normal operation mode (Normal mode/High-speed mode)
2) PROM serial programming mode
3) PROM parallel programming mode

The operating mode is decided by the XSPRG terminal setting at power on or initial reset.

Normal operation mode

In this mode, the E0C88 core CPU and the peripheral circuits operate by the programmed PROM. The CPU can enter this mode after the PROM programming has finished.
The PROM bit data is set to "1" at shipment. Therefore, the IC will not work even if the normal operation mode is set before programming.

In the normal operation mode, set the terminals for the PROM programmer as below. The board must be designed so that the terminal settings cannot be changed.

XSPRG: Fix at a High level.
RXD, SCLK, CLKW: Open or fix at a High level.
TXD: Open.

PROM serial programming mode

The PROM serial programming mode should be set when writing data to the PROM using a serial transfer from the exclusive PROM writer (UNIVERSAL ROM WRITER II). This mode will be used for the programming of chip products, because the programming can be done even when the IC has already been mounted on the board.
To create data to be written to the PROM, use the E0C88 assembler similar to the E0C88xxx.
The following explains the procedure of PROM serial programming.

<PROM serial programming procedure>

(1) Set the required terminals for serial programming as follows:

XSPRG: Set the terminal so that it will be fixed to a Low level. (A switch should be provided on the target board to change the XSPRG terminal level between High and Low.)

Note: The XSPRG terminal must be fixed at a Low level in the programming mode and at a High level in the normal operation mode. Changing the voltage level may damage the IC.

RXD, TXD, SCLK: Connect to the PROM writer.

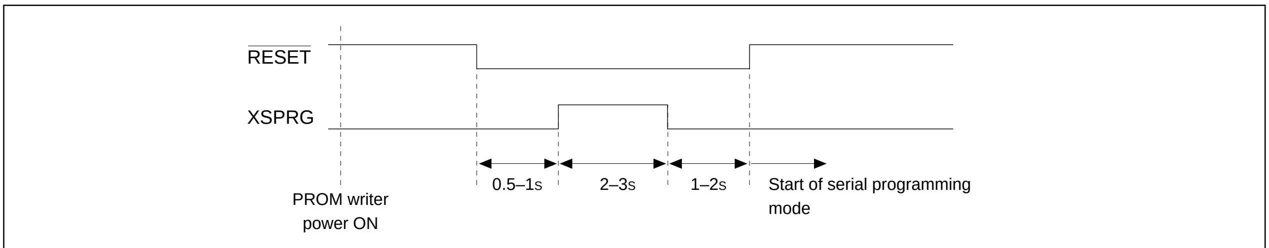
CLKW: Connect to the PROM writer. A 3.072 MHz clock will be supplied from the PROM writer at programming.

Other terminals should be set as below.
Input port (K) and I/O port (P) terminals: Fix at a High or Low level.
$\overline{\text{TEST}}$ terminal: Fix at a High level.

(2) Turn the IC (user target board) power (+5 V) on.
A power voltage must be supplied to the V_{DD} and V_{SS} terminals same as the regular operation so that the OSC1 oscillation circuits operate normally.

(3) Turn the PROM writer on.

(4) Controls the $\overline{\text{RESET}}$ and XSPRG terminals as shown below.



(5) Start up us88f360.exe or jp88f360.exe in the personal computer, then load the 88f360.frm file. This allows serial programming to begin.
After setting this mode, data can be written to the exclusive PROM writer (UNIVERSAL ROM WRITER II).
Refer to the "E0C88Pxxx Universal ROM Writer II User’s Manual" for the connection and operation of the PROM writer.

PROM parallel programming mode

In the PROM parallel programming mode, the exclusive PROM writer (UNIVERSAL ROM WRITER II) transfers data in parallel to the IC installed on the PROM writer to write data to it. The terminal setting is done by the PROM writer. Thus there is no precaution on mode setting or board design.
Refer to the "E0C88Pxxx Universal ROM Writer II User’s Manual" for the operation of the PROM writer.
To create data to be written to the PROM, use the E0C88 assembler the same as the E0C88xxx.

■ DIFFERENCES FROM THE MASK ROM MODELS

● Mask Option

The mask option items are fixed in the E0C88F360 as shown in the table below.

Mask option		Set 1	Set 2
OSC1 oscillation circuit		Crystal oscillation (32.768 kHz)	Crystal oscillation (32.768 kHz)
OSC3 oscillation circuit		CR oscillation	Crystal/ceramic oscillation
Multiple key entry reset combination		Not use	Not use
SVD reset		Not use	Not use
Input port pull up resistor	K00	With resistor	With resistor
	K01	With resistor	With resistor
	K02	With resistor	With resistor
	K03	With resistor	With resistor
	K04	With resistor	With resistor
	K05	With resistor	With resistor
	K06	With resistor	With resistor
	K07	With resistor	With resistor
	K10	With resistor	With resistor
	K11	With resistor	With resistor
	$\overline{\text{RESET}}$	With resistor	With resistor
I/O port pull up resistor	P00	With resistor	With resistor
	P01	With resistor	With resistor
	P02	With resistor	With resistor
	P03	With resistor	With resistor
	P04	With resistor	With resistor
	P05	With resistor	With resistor
	P06	With resistor	With resistor
	P07	With resistor	With resistor
	P10	With resistor	With resistor
	P11	With resistor	With resistor
	P12	With resistor	With resistor
	P13	With resistor	With resistor
	P14	No resistor	No resistor
	P15	No resistor	No resistor
	P16	No resistor	No resistor
	P17	No resistor	No resistor
Output port specification	R00	Complementary	Complementary
	R01	Complementary	Complementary
	R02	Complementary	Complementary
	R03	Complementary	Complementary
	R04	Complementary	Complementary
	R05	Complementary	Complementary
	R06	Complementary	Complementary
	R07	Complementary	Complementary
	R10	Complementary	Complementary
	R11	Complementary	Complementary
	R12	Complementary	Complementary
	R13	Complementary	Complementary
	R14	Complementary	Complementary
	R15	Complementary	Complementary
	R16	Complementary	Complementary
	R17	Complementary	Complementary
LCD drive duty		1/32 & 1/16 duty	1/32 & 1/16 duty
LCD power supply		Internal power supply (4.5 V)	Internal power supply (5.5 V)

● Power Supply

Operating voltage range

Model	Normal mode (V_{D1} = 2.2V)	High-speed mode (V_{D1} = 3.3V)	Low-power mode (V_{D1} = 1.6V)
E0C88F360	2.4 to 5.5V	3.5 to 5.5V	*1.8 to 3.5V
E0C88316	2.4 to 5.5V	3.5 to 5.5V	1.8 to 3.5V
E0C88317	2.4 to 5.5V	3.5 to 5.5V	1.8 to 3.5V
E0C88348	2.4 to 5.5V	3.5 to 5.5V	1.8 to 3.5V
E0C88308	2.4 to 5.5V	3.5 to 5.5V	1.8 to 3.5V
E0C88860	2.4 to 5.5V	3.5 to 5.5V	1.8 to 3.5V
E0C88861	2.4 to 5.5V	3.5 to 5.5V	1.8 to 3.5V
E0C88862	2.4 to 5.5V	3.5 to 5.5V	1.8 to 3.5V
E0C88832	2.4 to 5.5V	3.5 to 5.5V	1.8 to 3.5V

* The minimum operating voltage (1.8V) in Low-power mode is subject to change without notice.

The E0C88F360 operation is guaranteed within the above voltage range.

LCD drive voltage (V_{C1}–V_{C5})

LCD drive voltage	Condition		E0C883xx/888xx		E0C88F360	
			Min.	Max.	Min.	Max.
V_{C1}	*1		0.18V_{C5}	0.22V_{C5}	0.18V_{C5}	0.22V_{C5}
V_{C2}	*2		0.39V_{C5}	0.43V_{C5}	0.39V_{C5}	0.43V_{C5}
V_{C3}	*3		0.59V_{C5}	0.63V_{C5}	0.59V_{C5}	0.63V_{C5}
V_{C4}	*4		0.80V_{C5}	0.84V_{C5}	0.80V_{C5}	0.84V_{C5}
V_{C5} TYPE A (4.5 V)	*5	LCX = 0H	Typ. × 0.94	Typ. × 1.06	Typ. × 0.94	Typ. × 1.06
		LCX = 1H				
		LCX = 2H				
		LCX = 3H				
		LCX = 4H				
		LCX = 5H				
		LCX = 6H				
		LCX = 7H				
		LCX = 8H				
		LCX = 9H				
		LCX = AH				
		LCX = BH				
		LCX = CH				
		LCX = DH				
		LCX = EH				
		LCX = FH				
V_{C5} TYPE B (5.5 V)	*5	LCX = 0H	Typ. × 0.94	Typ. × 1.06	Typ. × 0.94	Typ. × 1.06
		LCX = 1H				
		LCX = 2H				
		LCX = 3H				
		LCX = 4H				
		LCX = 5H				
		LCX = 6H				
		LCX = 7H				
		LCX = 8H				
		LCX = 9H				
		LCX = AH				
		LCX = BH				
		LCX = CH				
		LCX = DH				
		LCX = EH				
		LCX = FH				

(Unit: V)

*1: when a 1 MΩ load resistor is connected between V_{SS} and V_{C1}
*2: when a 1 MΩ load resistor is connected between V_{SS} and V_{C2}
*3: when a 1 MΩ load resistor is connected between V_{SS} and V_{C3}
*4: when a 1 MΩ load resistor is connected between V_{SS} and V_{C4}
*5: when a 1 MΩ load resistor is connected between V_{SS} and V_{C5}

Initial Reset

E0C88F360 uses the initial reset signal as a trigger for setting either the normal operation mode or the programming mode. Therefore, design the reset input circuit so that the IC will be reset for sure. When resetting the IC in the normal operation mode, make sure to fix the XSPRG terminal at High level.

ROM

The E0C88F360 employs a Flash EEPROM for the internal ROM. The ROM has a capacity of 61,440 × 8 bits and is allocated to 000000H–00EFFFH. The Flash EEPROM can be rewritten up to 1,000 times. Rewriting data is done at the user's own risk.

RAM

The built-in RAM has a capacity of 2,048 words × 8 bits and is allocated to 00F000H–00F7FFH.

Oscillation Circuit

In the E0C88F360, only crystal oscillator is available for the OSC1 oscillation circuit and either CR or crystal/ceramic oscillator is available for the OSC3 oscillation circuit. Furthermore, pay attention to the difference on the oscillation start time according to the supply voltage. Be sure to have enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

SVD Circuit

The E0C88F360 has a built-in SVD circuit.

Detection level	E0C883xx/888xx			E0C883F360		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Level 1 → Level 0	Typ. × 0.92	1.82	Typ. × 1.08	Typ. × 0.92	1.82	Typ. × 1.08
Level 2 → Level 1		2.00			2.00	
Level 3 → Level 2		2.18			2.18	
Level 4 → Level 3		2.36			2.36	
Level 5 → Level 4		2.54			2.54	
Level 6 → Level 5		2.72			2.72	
Level 7 → Level 6		2.90			2.90	
Level 8 → Level 7		3.08			3.08	
Level 9 → Level 8		3.26			3.26	
Level 10 → Level 9	Typ. × 0.88	3.45	Typ. × 1.12	Typ. × 0.88	3.45	Typ. × 1.12
Level 11 → Level 10		3.65			3.65	
Level 12 → Level 11		3.85			3.85	
Level 13 → Level 12		4.05			4.05	
Level 14 → Level 13		4.25			4.25	
Level 15 → Level 14		4.50			4.50	

(Unit: V)

The mask option for reseting when low voltage is detected (available in the E0C88xxx) is not provided in the E0C88F360.

● List of Different Specifications between E0C88F360 and E0C88xxx

			E0C88348	E0C88316/317	E0C88308	E0C88862	E0C88861	E0C88832	E0C88F360	E0C88P348
Package	QFP18-176pin		×	×	×	×	×	×	○	○
	QFP8-160pin		○	○	○	×	×	×	×	○
	QFP8-128pin		×	×	×	○	○	○	×	×
	QFP15-128pin		×	×	×	○	○	○	×	×
Number of additional pin for Flash			–	–	–	–	–	–	5 pins	5 pins
ROM size			48KB	16KB	8KB	60KB	60KB	32KB	60KB	48KB
RAM size			2KB	2KB	256B	1.5KB	1.5KB	1.5KB	2KB	2KB
Input port			10	←	9	←	←	←	10	10
Output port			9	←	5	2	2	2	9	9
I/O port			8	←	←	←	←	←	8	8
Chip mode	Single chip		○	○	○	○	○	○	○	○
	Extended 64K	MCU	×	○	○	○	○	○	×	×
		MPU	○	○	○	○	○	○	○	×
	Extended 512K min.	MCU	○	○	○	○	○	○	○	○
		MPU	○	○	○	○	○	○	○	×
	Extended 512K max.	MCU	○	○	○	○	○	○	○	○
		MPU	○	○	○	○	○	○	○	×
Operating mode	Normal	(V_{D1} = 2.2V)	○	○	○	○	○	○	○	○
	High-speed	(V_{D1} = 3.3V)	○	○	○	○	○	○	○	○
	Low-power	(V_{D1} = 1.3V)	○	○	○	○	○	○	○	×
Mask ROM option select	OSC1	Crystal	○	○	○	○	○	○	○	○
		External	○	○	○	○	○	○	×	×
		CR	○	○	○	○	○	○	×	×
		Crystal (with C_G)	○	○	○	○	○	○	×	×
	OSC3	Crystal	○	○	○	○	○	○	○	○
		Ceramic	○	○	○	○	○	○	○	○
		CR	○	○	○	○	○	○	○	×
		External	○	○	○	○	○	○	×	×
	I/O (P) port pull-up	With resistor	○	○	○	○	○	○	○	○
		Gate direct	○	○	○	○	○	○	×	×
	Input (K) port pull-up	With resistor	○	○	○	○	○	○	○	○
		Gate direct	○	○	○	○	○	○	×	×
	Output (R) port output spec.	Complementary	○	○	○	○	○	○	○	○
		Nch open drain	○	○	○	○	○	○	×	×
	LCD duty	1/32 & 1/16	○	○	○	○	○	○	○	○
		1/8	○	○	○	○	○	○	×	×
	LCD power	TYPE A (4.5V)	○	○	○	○	○	○	○	×
		TYPE B (5.5V)	○	○	○	○	○	○	○	○
		External power source	○	○	○	○	○	○	×	×
	Reset	K0 port combination	○	○	○	○	○	○	×	×
		SVD reset	○	○	○	○	○	○	×	×
Operating voltage		Normal	2.4 ~ 5.5V	←	←	←	←	←	←	3.3 ~ 5.5V
		High-speed	3.5 ~ 5.5V	←	←	←	←	←	←	4.5 ~ 5.5V
		Low-power	1.8 ~ 3.5V	←	←	←	←	←	← *1	×
Operating frequency	OSC1	Normal	30k ~ 50kHz	←	←	←	←	←	←	←
		High-speed	30k ~ 50kHz	←	←	←	←	←	←	←
		Low-power	30k ~ 50kHz	←	←	←	←	←	←	×
	OSC3	Normal	30k ~ 4.1MHz	←	←	←	←	←	←	←
		High-speed	30k ~ 8.2MHz	←	←	←	←	←	←	30k ~ 6MHz
Operating temperature			-40 ~ 85°C	←	←	←	←	←	-20 ~ 70°C	0 ~ 70°C
Power current (max.)	Normal (5.5V, 32kHz)		18µA	←	←	TBD	TBD	TBD	25µA	12mA
	High-speed (5.5V, 1MHz)		1.0mA	←	←	TBD	TBD	TBD	2.0mA	15mA
	Sleep mode (5.5V, normal mode)		1µA	←	←	TBD	TBD	TBD	1µA	1µA
Power supply	CPU		V_{D1}	←	←	←	←	←	←	V_{DD}
	Peripheral		V_{D1}	←	←	←	←	←	←	V_{DD}
	Port		V_{DD}	←	←	←	←	←	←	←
	OSC		V_{D1}	←	←	V_{OSC}	V_{D1}	←	←	←
	PROM		×	×	×	×	×	×	V_{D1}	V_{DD}
SVD			16 levels	←	←	←	←	←	←	8 levels
Analog comparator			2 ch.	←	←	×	×	×	2 ch.	×
A/D converter			×	×	×	×	×	×	4 ch., 10 bits	×
R26 output port specification			R26/FR	R26/FR	R26/FR	R26/$\overline{\text{TOUT}}$	R26/$\overline{\text{TOUT}}$	R26/$\overline{\text{TOUT}}$	R26/FR/$\overline{\text{TOUT}}$	R26/FR
R51 output port specification			R51/$\overline{\text{BACK}}$	R51/$\overline{\text{BACK}}$	R51/$\overline{\text{BACK}}$	R51/$\overline{\text{BZ}}$	R51/$\overline{\text{BZ}}$	R51/$\overline{\text{BZ}}$	R51/$\overline{\text{BACK}}$/$\overline{\text{BZ}}$	R51/$\overline{\text{BACK}}$

○ = Available, × = Not available

*1: The E0C88F360 operating voltage range (1.8V to 3.5V) in Low-power mode may be modified.

Notes:
- The pin assignment of the E0C88F360 is incompatible with the E0C883xx and E0C888xx.
- The table does not contain some different items. Refer to the manuals of the E0C88F360 and the E0C88xxx.

■ SUMMARY OF NOTES

● Notes Related to the PROM

(1) The PROM data bit is set to "1" at shipment. Therefore, It must be programmed before operating the IC in the normal operation mode.

(2) The PROM data can be rewritten up to 1,000 times. (Decrement the count every time the PROM is erased and written.)

(3) The circuit board should be designed so that the terminals can switch the input signals that differ between the PROM serial programming mode and the normal operation mode.

(4) The terminals for the PROM programmer should be set correctly according to the operating mode and fixed so that they cannot be changed during operation. Especially the XSPRG terminal must be fixed at a Low level in the programming mode, while they must be fixed at a High level in the normal operation mode. Changing the voltage level may damage the IC.

(5) If the operation of the E0C88F360 is unstable even though the writing and verification of the PROM data was completed normally, write and verify the PROM data without erasing the PROM.

(6) Rewriting the PROM is done at on the user's own risk.

● Notes on Differences form the E0C883xx and E0C888xx

Be aware of the following notes when using the E0C88F360 as a development tool for the E0C883xx or E0C888xx.

Memory

The E0C88F360 contains a ROM and RAM lager than most of all E0C883xx/E0C888xx models. When developing an application, pay attention to the memory size.

Power supply

The E0C88F360 is operable with a supply voltage within the range of 1.8 V to 5.5 V. Be aware that as the supply voltage is different from the E0C883xx/E0C888xx the electrical characteristics differ. Refer to Electrical Characteristics.

Initial reset

Note that the power-on reset time differs from the E0C883xx/E0C888xx because the supply voltage is different.

Oscillation circuit

In the E0C88F360, a crystal oscillator can only be used for the OSC1 oscillation circuit and a CR or crystal/ ceramic oscillator for the OSC3 oscillation circuit. Furthermore, pay attention to the difference on the oscillation start time according to the supply voltage. Be sure there is enough margin especially for stabilizing the OSC3 oscillation when controlling the peripheral circuit that uses the OSC3 clock.

LCD controller

The LCD drive voltage range of the E0C88F360 is different from that of the E0C883xx/E0C888xx. Check the electrical characteristic differences by referring to the E0C88F360 and E0C883xx/E0C888xx Technical Manuals before designing the LCD unit. Moreover, note that because mask options are fixed, the LCD drive duty of the E0C88F360 is fixed at 1/32 or 1/16 duty. The internal LCD power supply can be selected either 4.5 V or 5.5 V.

Mask option

In the E0C88F360, some mask options for the E0C883xx/E0C888xx are fixed. Therefore, some optional functions cannot be used in the E0C88F360. Check whether the functions are enabled or not in the E0C88F360 and E0C883xx/E0C888xx Technical Manuals.

A/D converter and analog comparator

Note that the A/D converter and the analog comparator cannot be used at the same time.

■ ELECTRICAL CHARACTERISTICS

Note: The electrical characteristics of the E0C88F360 are different from those of the E0C883xx/E0C888xx. The following characteristics should be used as reference values when using the E0C88F360 as a development tool.

● Absolute Maximum Rating

(V_{SS}=0V)

Item	Symbol	Condition	Value	Unit	Note
Power voltage	V_{DD}		-0.3 to +7.0	V	
Liquid crystal power voltage	V_{C5}		-0.3 to +7.0	V	
Input voltage	V_I		-0.3 to V_{DD} + 0.3	V	
Output voltage	V_O		-0.3 to V_{DD} + 0.3	V	
High level output current	I_{OH}	1 terminal	-5	mA	
		Total of all terminals	-20	mA	
Low level output current	I_{OL}	1 terminal	5	mA	
		Total of all terminals	20	mA	
Permitted loss	P_D		200	mW	1
Operating temperature	Topr		-20 to 70	°C	
Storage temperature	Tstg		-65 to +150	°C	2

Note) 1 In case of plastic package.
2 This rated value cannot insure the PROM data holding function.

● Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Operating power voltage (Normal)	V_{DD}		2.4		5.5	V	
Operating power voltage (High-speed)	V_{DD}		3.5		5.5	V	
Operating power voltage (Low-power)	V_{DD}		1.8 *		3.5	V	5
Operating frequency (Normal)	f_{OSC1}	V_{DD} = 2.4 to 3.5V	30.000	32.768	50.000	kHz	
	f_{OSC3}		0.03		4.2	MHz	
Operating frequency (High-speed)	f_{OSC1}	V_{DD} = 3.5 to 5.5V	30.000	32.768	50.000	kHz	
	f_{OSC3}		0.03		8.2 *	MHz	5
LCD power voltage	V_{C5}				7.0	V	
Capacitor between V_{D1} and V_{SS}	C_1			0.1		µF	3
Capacitor between V_{C1} and V_{SS}	C_2			0.1		µF	3
Capacitor between V_{C2} and V_{SS}	C_3			0.1		µF	3
Capacitor between V_{C3} and V_{SS}	C_4			0.1		µF	3
Capacitor between V_{C4} and V_{SS}	C_5			0.1		µF	3
Capacitor between V_{C5} and V_{SS}	C_6			0.1		µF	3
Capacitor between CA and CB	C_7			0.1		µF	3
Capacitor between CA and CC	C_8			0.1		µF	3
Capacitor between CD and CE	C_9			0.1		µF	3
Resistor between V_{C1} and V_{SS}	R_1			100		kΩ	4

Note) 3 No capacitor is required when the LCD power supply is not used. In this case, leave the V_{C1}–V_{C5} and CA–CE terminals open.
4 It is necessary when the panel load is large and for 1/32 duty driving.
The resistance value should be decided by connecting it to the actual panel to be used.
5 The value with * may change without norice. It will affect the related characteristics.

● DC Characteristics

(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
High level input voltage	V_{IH}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW, MCU/$\overline{\text{MPU}}$	0.8V_{DD}		V_{DD}	V	
Low level input voltage	V_{IL}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW, MCU/$\overline{\text{MPU}}$	0		0.2V_{DD}	V	
High level schmitt input voltage	V_{T+}	$\overline{\text{RESET}}$	0.5V_{DD}		0.9V_{DD}	V	
Low level schmitt input voltage	V_{T-}	$\overline{\text{RESET}}$	0.1V_{DD}		0.5V_{DD}	V	
High level output current	I_{OH}	Pxx, Rxx, TXD, V_{OH} = 0.9V_{DD}			-0.5	mA	
Low level output current	I_{OL}	Pxx, Rxx, TXD, V_{OL} = 0.1V_{DD}	0.5			mA	
Input leak current	I_{LI}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW, $\overline{\text{RESET}}$, MCU/$\overline{\text{MPU}}$	-1		1	µA	
Output leak current	I_{LO}	Pxx, Rxx, TXD	-1		1	µA	
Input pull-up resistance	R_{IN}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW, $\overline{\text{RESET}}$, MCU/$\overline{\text{MPU}}$	100		500	kΩ	
Input terminal capacitance	C_{IN}	Kxx, Pxx, XSPRG, RXD, SCLK, CLKW			15	pF	
Segment/Common output current	I_{SEGH}	SEGxx, COMxx, V_{SEGH} = V_{C5}-0.1V			-5	µA	
	I_{SEGL}	SEGxx, COMxx, V_{SEGL} = 0.1V	5			µA	

● Analog Circuit Characteristics

LCD drive circuit

(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C, C_1–C_9=0.1µF)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Note
LCD drive voltage	V_{C1}	#1		0.18V_{C5}		0.22V_{C5}	V	
	V_{C2}	#2		0.39V_{C5}		0.43V_{C5}	V	
	V_{C3}	#3		0.59V_{C5}		0.63V_{C5}	V	
	V_{C4}	#4		0.80V_{C5}		0.84V_{C5}	V	
	V_{C5} TYPE A (4.5V)	#5	LCX = 0H		3.89		V	
			LCX = 1H		3.96		V	
			LCX = 2H		4.04		V	
			LCX = 3H		4.11		V	
			LCX = 4H		4.18		V	
			LCX = 5H		4.26		V	
			LCX = 6H		4.34		V	
			LCX = 7H	Typ×0.94	4.42	Typ×1.06	V	
			LCX = 8H		4.50		V	
			LCX = 9H		4.58		V	
			LCX = AH		4.66		V	
			LCX = BH		4.74		V	
			LCX = CH		4.82		V	
			LCX = DH		4.90		V	
			LCX = EH		4.99		V	
			LCX = FH		5.08		V	
	V_{C5} TYPE B (5.5V)	#5	LCX = 0H		4.73		V	
			LCX = 1H		4.83		V	
			LCX = 2H		4.92		V	
			LCX = 3H		5.02		V	
			LCX = 4H		5.11		V	
			LCX = 5H		5.21		V	
			LCX = 6H		5.30		V	
			LCX = 7H	Typ×0.94	5.40	Typ×1.06	V	
			LCX = 8H		5.50		V	
			LCX = 9H		5.60		V	
			LCX = AH		5.70		V	
			LCX = BH		5.81		V	
			LCX = CH		5.93		V	
			LCX = DH		6.05		V	
			LCX = EH		6.17		V	
			LCX = FH		6.29		V	

#1 Connects 1MΩ load resistor between V_{SS} and V_{C1}.
#2 Connects 1MΩ load resistor between V_{SS} and V_{C2}.
#3 Connects 1MΩ load resistor between V_{SS} and V_{C3}.
#4 Connects 1MΩ load resistor between V_{SS} and V_{C4}.
#5 Connects 1MΩ load resistor between V_{SS} and V_{C5}.

SVD circuit

(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
SVD voltage	V_{SVD}	Level 1 → Level 0		1.82		V	6
		Level 2 → Level 1		2.00		V	6
		Level 3 → Level 2		2.18		V	6
		Level 4 → Level 3		2.36		V	6
		Level 5 → Level 4	Typ×0.92	2.54	Typ×1.08	V	7
		Level 6 → Level 5		2.72		V	7
		Level 7 → Level 6		2.90		V	7
		Level 8 → Level 7		3.08		V	7
		Level 9 → Level 8		3.26		V	7
		Level 10 → Level 9		3.45		V	7
		Level 11 → Level 10		3.65		V	8
		Level 12 → Level 11	Typ×0.88	3.85	Typ×1.12	V	8
		Level 13 → Level 12		4.05		V	8
		Level 14 → Level 13		4.25		V	8
		Level 15 → Level 14		4.50		V	8

V_{SVD} (Level 0) < V_{SVD} (Level 1) < V_{SVD} (Level 2) < V_{SVD} (Level 3) < V_{SVD} (Level 4) < V_{SVD} (Level 5) < V_{SVD} (Level 6) < V_{SVD} (Level 7) < V_{SVD} (Level 8) < V_{SVD} (Level 9) < V_{SVD} (Level 10) < V_{SVD} (Level 11) < V_{SVD} (Level 12) < V_{SVD} (Level 13) < V_{SVD} (Level 14) < V_{SVD} (Level 15)

Note) 6 Low-power operation mode
7 Low-power or normal operation mode
8 Normal or high-speed operating mode

Analog comparator

(Unless otherwise specified: V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Analog comparator operating voltage input range	V_{CMIP}	Non-inverted input (CMPP)	0.7		V_{DD} - 0.7	V	9
	V_{CMIM}	Inverted input (CMPM)	0.7		V_{DD} - 0.7	V	9
Analog comparator offset voltage	V_{CMOF}	V_{CMIP} = 0.7V to V_{DD} - 0.7V V_{CMIM} = 0.7V to V_{DD} - 0.7V			20	mV	9
Analog comparator stability time	t_{CMP1}				1	mS	10
Analog comparator response time	t_{CMP2}	V_{CMIP} = 0.7V to V_{DD} - 0.7V V_{CMIM} = 0.7V to V_{DD} - 0.7V V_{CMIP} = V_{CMIM} ± 0.025V			2	mS	11

Note) 9 When "no pull-up resistor" (comparator input terminal) is selected by mask option.
10 Stability time is the time from turning the circuit ON until the circuit is stabilized.
11 Response time is the time that the output result responds to the input signal.

A/D converter

(Unless otherwise specified: V_{DD}=AV_{DD}=AV_{REF}=5.0V, V_{SS}=AV_{SS}=0V, f_{OSC1}=32.768kHz, f_{OSC3}=4.0MHz, Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Zero-scale error	Ezs	V_{DD}=AV_{DD}=AV_{REF}=2.7 to 5.5V, ADCLK=2MHz, Ta=25°C	-1.50		1.50	LSB	
Full-scale error	Efs		-1.50		1.50	LSB	
Non-linearity error	El		-1.50		1.50	LSB	
Total error	Et		-3.00		3.00	LSB	
A/D converter current consumption	I_{AD}	V_{DD}=AV_{DD}=AV_{REF}=3.0V, ADCLK=2MHz, Ta=25°C AV_{REF} and ADCLK divider current not included		0.50	1.00	mA	
		V_{DD}=AV_{DD}=AV_{REF}=5.0V, ADCLK=2MHz, Ta=25°C AV_{REF} and ADCLK divider current not included		1.80	3.50	mA	
Input clock frequency	f	V_{DD}=AV_{DD}=AV_{REF}=2.7 to 5.5V, Ta=25°C		2	4	MHz	

* Zero-scale error: Ezs = deviation from the ideal value at zero point
* Full-scale error: Efs = deviation from the ideal value at the full scale point
* Non-linearity error: El = deviation of the real conversion curve from the end point line
* Total error: Et = max(Ezs, Efs, Eabs), Eabs = deviation from the ideal line (including quantization error)

● Power Current Consumption (The table shows objective values, so they may be changed.)

(Unless otherwise specified: V_{DD}=Within the operating voltage in each operating mode, V_{SS}=0V, Ta=25°C, OSC1=32.768kHz crystal oscillation, C_G=25pF, OSC3=External clock input, Non heavy load protection mode, C_1–C_9=0.1µF, No panel load)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power current (Normal mode)	I_{DD1}	In SLEEP status #1			1	µA	
	I_{DD2}	In HALT status #2		3	5	µA	
	I_{DD3}	CPU is in RUN status (V_{DD} = 5.5V, 32.768kHz) #3		18	25	µA	
	I_{DD4}	CPU is in RUN status (V_{DD} = 5.5V, 1MHz) #4		0.5	1	mA	
	I_{HVL}	In heavy load protection mode			70	µA	12
Power current (High-speed mode)	I_{DD1}	In SLEEP status #1			3	µA	
	I_{DD2}	In HALT status #2			10	µA	
	I_{DD3}	CPU is in RUN status (V_{DD} = 5.5V, 32.768kHz) #3		32	40	µA	
	I_{DD4}	CPU is in RUN status (V_{DD} = 5.5V, 1MHz) #4		1	2	mA	
	I_{HVL}	In heavy load protection mode			100	µA	12
Power current (Low-power mode)	I_{DD1}	In SLEEP status #1			1	µA	
	I_{DD2}	In HALT status #2			5	µA	
	I_{DD3}	CPU is in RUN status (V_{DD} = 3.5V, 32.768kHz) #3		10	16	µA	
	I_{HVL}	In heavy load protection mode			40	µA	12
LCD drive circuit current	I_{LCDN}	V_{DD} = 5.5V			8	µA	
	I_{LCDH}	In heavy load protection mode			35	µA	12
SVD circuit current	I_{SVDN}	V_{DD} = 5.5V			180	µA	13
	I_{SVDH}	In heavy load protection mode			240	µA	12
Analog comparator circuit current	I_{CMP1}	CMPXDT="1"			100	µA	
	I_{CMP2}	CMPXDT="0"			10	µA	

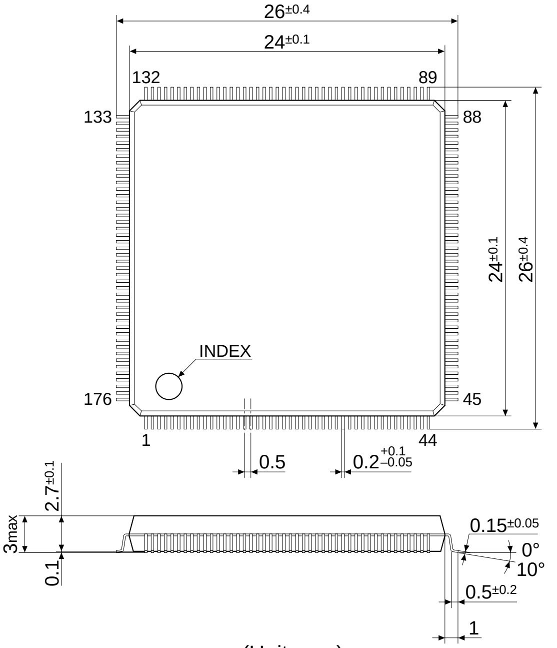
#1 OSC1: Stop, OSC3: Stop, CPU, ROM, RAM: SLEEP status, Clock timer: Stop, Others: Stop status
#2 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: HALT status, Clock timer: Runing, Others: Stop status
#3 OSC1: Oscillating, OSC3: Stop, CPU, ROM, RAM: Runing in 32.768kHz, Clock timer: Runing, Others: Stop status
#4 OSC1: Oscillating, OSC3: Oscillating, CPU, ROM, RAM: Runing in 1MHz, Clock timer: Runing, Others: Stop status

Note) 12 It is the value of current which flows in the heavy load protection circuit when in the heavy load protection mode (OSC3 ON or buzzer ON).
13 The value when V_{DD} = x V can be found by the following expression: I_{SVDN} (V_{DD} = x V) = ($x \times 60$) - 150 (Max. value)
In the E0C88F360, CR option cannot be selected for the OSC1 oscillation circuit.

■ PACKAGE AND PAD LAYOUT

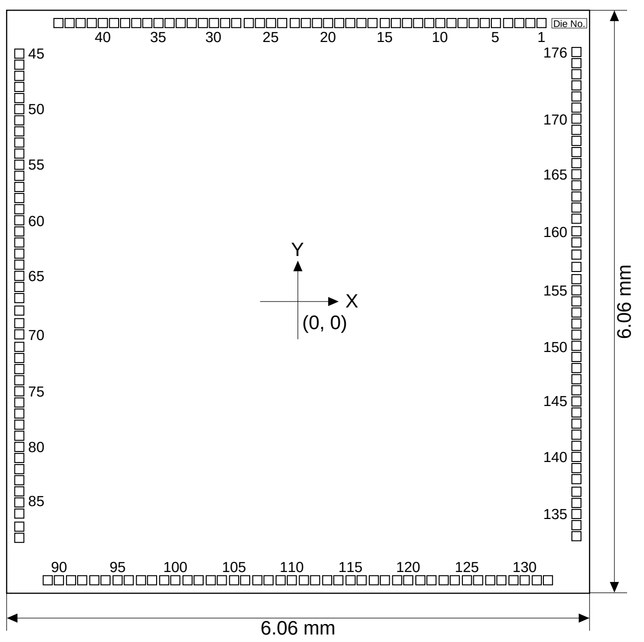
● Package Dimensions

Plastic QFP18-176pin



(Unit: mm)
The dimensions are subject to change without notice.

● Diagram of Pad Layout



Chip thickness: 400 µm
Pad opening: 95 µm

● Pin Layout (QFP18-176pin)

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	SEG2	37	SEG38	73	CE	109	P12/SCLK	145	R25/CL
2	SEG3	38	SEG39	74	CD	110	P11/SOUT	146	R26/FR
3	SEG4	39	SEG40	75	CC	111	P10/SIN	147	R27/TOUT
4	SEG5	40	SEG41	76	CB	112	AV_{DD}	148	R30/$\overline{\text{CE0}}$
5	SEG6	41	SEG42	77	CA	113	AV_{SS}	149	R31/$\overline{\text{CE1}}$
6	SEG7	42	SEG43	78	V_{C5}	114	AV_{REF}	150	R32/$\overline{\text{CE2}}$
7	SEG8	43	SEG44	79	V_{C4}	115	V_{DD}	151	R33/$\overline{\text{CE3}}$
8	SEG9	44	SEG45	80	V_{C3}	116	P07/D7	152	R34/FOUT
9	SEG10	45	SEG46	81	V_{C2}	117	P06/D6	153	R35
10	SEG11	46	SEG47	82	V_{C1}	118	P05/D5	154	R36
11	SEG12	47	SEG48	83	OSC3	119	P04/D4	155	R37
12	SEG13	48	SEG49	84	OSC4	120	P03/D3	156	V_{SS}
13	SEG14	49	SEG50	85	V_{D1}	121	P02/D2	157	COM0
14	SEG15	50	COM31/SEG51	86	V_{DD}	122	P01/D1	158	COM1
15	SEG16	51	COM30/SEG52	87	V_{SS}	123	P00/D0	159	COM2
16	SEG17	52	COM29/SEG53	88	V_{OSC}	124	R00/A0	160	COM3
17	SEG18	53	COM28/SEG54	89	OSC1	125	R01/A1	161	COM4
18	SEG19	54	COM27/SEG55	90	OSC2	126	R02/A2	162	COM5
19	SEG20	55	COM26/SEG56	91	$\overline{\text{TEST}}$	127	R03/A3	163	COM6
20	SEG21	56	COM25/SEG57	92	$\overline{\text{RESET}}$	128	R04/A4	164	COM7
21	SEG22	57	COM24/SEG58	93	MCU/$\overline{\text{MPU}}$	129	R05/A5	165	COM8
22	SEG23	58	COM23/SEG59	94	K11/BREQ	130	R06/A6	166	COM9
23	SEG24	59	COM22/SEG60	95	K10/EVIN	131	R07/A7	167	COM10
24	SEG25	60	COM21/SEG61	96	K07	132	R10/A8	168	COM11
25	SEG26	61	COM20/SEG62	97	K06	133	R11/A9	169	COM12
26	SEG27	62	COM19/SEG63	98	K05	134	R12/A10	170	COM13
27	SEG28	63	COM18/SEG64	99	K04	135	R13/A11	171	COM14
28	SEG29	64	COM17/SEG65	100	K03	136	R14/A12	172	COM15
29	SEG30	65	COM16/SEG66	101	K02	137	R15/A13	173	R50/BZ
30	SEG31	66	V_{D1F}	102	K01	138	R16/A14	174	R51/$\overline{\text{BACK}}$
31	SEG32	67	XSPRG	103	K00	139	R17/A15	175	SEG0
32	SEG33	68	CLKW	104	P17/CMPM1	140	R20/A16	176	SEG1
33	SEG34	69	VEPEXT	105	P16/CMPP1	141	R21/A17	–	–
34	SEG35	70	RXD	106	P15/CMPM0	142	R22/A18	–	–
35	SEG36	71	SCLK	107	P14/CMPP0	143	R23/$\overline{\text{RD}}$	–	–
36	SEG37	72	TXD	108	P13/$\overline{\text{SRDY}}$	144	R24/$\overline{\text{WR}}$	–	–

● Pad Coordinates

(Unit: µm)

Pad		Coordinate		Pad		Coordinate		Pad		Coordinate	
No.	Name	x	x	No.	Name	x	x	No.	Name	x	x
1	OSC1	2,533	2,896	60	R30/$\overline{\text{CE0}}$	-2,896	846	119	SEG32	1,032	-2,896
2	OSC2	2,417	2,896	61	R31/$\overline{\text{CE1}}$	-2,896	730	120	SEG33	1,147	-2,896
3	$\overline{\text{TEST}}$	2,302	2,896	62	R32/$\overline{\text{CE2}}$	-2,896	615	121	SEG34	1,274	-2,896
4	$\overline{\text{RESET}}$	2,186	2,896	63	R33/$\overline{\text{CE3}}$	-2,896	499	122	SEG35	1,389	-2,896
5	MCU/$\overline{\text{MPU}}$	2,059	2,896	64	R34/FOUT	-2,896	384	123	SEG36	1,516	-2,896
6	K11/BREQ	1,943	2,896	65	R35	-2,896	268	124	SEG37	1,631	-2,896
7	K10/EVIN	1,828	2,896	66	R36	-2,896	153	125	SEG38	1,758	-2,896
8	K07	1,712	2,896	67	R37	-2,896	37	126	SEG39	1,874	-2,896
9	K06	1,597	2,896	68	V_{SS}	-2,896	-93	127	SEG40	2,000	-2,896
10	K05	1,481	2,896	69	R50/BZ	-2,896	-224	128	SEG41	2,116	-2,896
11	K04	1,366	2,896	70	R51/$\overline{\text{BACK}}$	-2,896	-340	129	SEG42	2,242	-2,896
12	K03	1,250	2,896	71	COM0	-2,896	-470	130	SEG43	2,358	-2,896
13	K02	1,135	2,896	72	COM1	-2,896	-586	131	SEG44	2,484	-2,896
14	K01	1,019	2,896	73	COM2	-2,896	-701	132	SEG45	2,600	-2,896
15	K00	904	2,896	74	COM3	-2,896	-817	133	SEG46	2,896	-2,456
16	P17/CMPM1	776	2,896	75	COM4	-2,896	-932	134	SEG47	2,896	-2,341
17	P16/CMPP1	661	2,896	76	COM5	-2,896	-1,048	135	SEG48	2,896	-2,214
18	P15/CMPM0	545	2,896	77	COM6	-2,896	-1,163	136	SEG49	2,896	-2,099
19	P14/CMPP0	430	2,896	78	COM7	-2,896	-1,279	137	SEG50	2,896	-1,976
20	P13/$\overline{\text{SRDY}}$	314	2,896	79	COM8	-2,896	-1,394	138	COM31/SEG51	2,896	-1,845
21	P12/$\overline{\text{SCLK}}$	199	2,896	80	COM9	-2,896	-1,510	139	COM30/SEG52	2,896	-1,730
22	P11/SOUT	83	2,896	81	COM10	-2,896	-1,625	140	COM29/SEG53	2,896	-1,614
23	P10/SIN	-32	2,896	82	COM11	-2,896	-1,741	141	COM28/SEG54	2,896	-1,499
24	AV_{DD}	-163	2,896	83	COM12	-2,896	-1,856	142	COM27/SEG55	2,896	-1,383
25	AV_{SS}	-279	2,896	84	COM13	-2,896	-1,972	143	COM26/SEG56	2,896	-1,268
26	AV_{REF}	-394	2,896	85	COM14	-2,896	-2,087	144	COM25/SEG57	2,896	-1,152
27	V_{DD}	-510	2,896	86	COM15	-2,896	-2,203	145	COM24/SEG58	2,896	-1,037
28	P07/D7	-641	2,896	87	SEG0	-2,896	-2,339	146	COM23/SEG59	2,896	-921
29	P06/D6	-756	2,896	88	SEG1	-2,896	-2,455	147	COM22/SEG60	2,896	-806
30	P05/D5	-872	2,896	89	SEG2	-2,600	-2,896	148	COM21/SEG61	2,896	-690
31	P04/D4	-987	2,896	90	SEG3	-2,484	-2,896	149	COM20/SEG62	2,896	-575
32	P03/D3	-1,103	2,896	91	SEG4	-2,358	-2,896	150	COM19/SEG63	2,896	-459
33	P02/D2	-1,218	2,896	92	SEG5	-2,242	-2,896	151	COM18/SEG64	2,896	-344
34	P01/D1	-1,334	2,896	93	SEG6	-2,116	-2,896	152	COM17/SEG65	2,896	-228
35	P00/D0	-1,449	2,896	94	SEG7	-2,000	-2,896	153	COM16/SEG66	2,896	-113
36	R00/A0	-1,565	2,896	95	SEG8	-1,874	-2,896	154	V_{D1F}	2,896	3
37	R01/A1	-1,680	2,896	96	SEG9	-1,758	-2,896	155	XSPRG	2,896	118
38	R02/A2	-1,796	2,896	97	SEG10	-1,631	-2,896	156	CLKW	2,896	234
39	R03/A3	-1,911	2,896	98	SEG11	-1,516	-2,896	157	VEPEXT	2,896	361
40	R04/A4	-2,027	2,896	99	SEG12	-1,389	-2,896	158	RXD	2,896	489
41	R05/A5	-2,142	2,896	100	SEG13	-1,274	-2,896	159	SCLK	2,896	616
42	R06/A6	-2,258	2,896	101	SEG14	-1,147	-2,896	160	TXD	2,896	732
43	R07/A7	-2,373	2,896	102	SEG15	-1,032	-2,896	161	CE	2,896	862
44	R10/A8	-2,489	2,896	103	SEG16	-905	-2,896	162	CD	2,896	978
45	R11/A9	-2,896	2,578	104	SEG17	-790	-2,896	163	CC	2,896	1,093
46	R12/A10	-2,896	2,463	105	SEG18	-663	-2,896	164	CB	2,896	1,209
47	R13/A11	-2,896	2,347	106	SEG19	-548	-2,896	165	CA	2,896	1,324
48	R14/A12	-2,896	2,232	107	SEG20	-421	-2,896	166	V_{C5}	2,896	1,440
49	R15/A13	-2,896	2,116	108	SEG21	-305	-2,896	167	V_{C4}	2,896	1,555
50	R16/A14	-2,896	2,001	109	SEG22	-179	-2,896	168	V_{C3}	2,896	1,671
51	R17/A15	-2,896	1,885	110	SEG23	-63	-2,896	169	V_{C2}	2,896	1,786
52	R20/A16	-2,896	1,770	111	SEG24	63	-2,896	170	V_{C1}	2,896	1,902
53	R21/A17	-2,896	1,654	112	SEG25	179	-2,896	171	OSC3	2,896	2,017
54	R22/A18	-2,896	1,539	113	SEG26	305	-2,896	172	OSC4	2,896	2,133
55	R23/$\overline{\text{RD}}$	-2,896	1,423	114	SEG27	421	-2,896	173	V_{D1}	2,896	2,248
56	R24/$\overline{\text{WR}}$	-2,896	1,308	115	SEG28	548	-2,896	174	V_{DD}	2,896	2,364
57	R25/CL	-2,896	1,192	116	SEG29	663	-2,896	175	V_{SS}	2,896	2,479
58	R26/FR	-2,896	1,077	117	SEG30	790	-2,896	176	V_{OSC}	2,896	2,595
59	R27/TOUT	-2,896	961	118	SEG31	905	-2,896	–			

■ PIN DESCRIPTION

Pin name	Pin No.	Pad No.	In/Out	Function
V_{DD}	86, 115	27, 174	–	Power supply (+) terminal
V_{SS}	87, 156	68, 175	–	Power supply (GND) terminal
V_{D1}	85	173	–	Internal logic system voltage regulator output terminal
V_{D1F}	66	154	–	Internal logic/Flash block voltage regulator output terminal (Normal: $V_{D1F}=V_{D1}$)
V_{OSC}	88	176	–	Oscillation voltage regulator output terminal
V_{C1}–V_{C5}	82–78	170–166	O	LCD drive voltage output terminals
CA–CE	77–73	165–161	–	Booster capacitor connection terminals for LCD
OSC1	89	1	I	OSC1 crystal oscillation input terminal
OSC2	90	2	O	OSC1 crystal oscillation output terminal
OSC3	83	171	I	OSC3 ceramic or CR oscillation input terminal
OSC4	84	172	O	OSC3 ceramic or CR oscillation output terminal
MCU/$\overline{\text{MPU}}$	93	5	I	Terminal for setting MCU or MPU modes
K00–K07	103–96	15–8	I	Input terminals (K00–K07)
K10/EVIN	95	7	I	Input terminal (K10) or event counter external clock input terminal (EVIN)
K11/$\overline{\text{BREQ}}$	94	6	I	Input terminal (K11) or bus request signal input terminal ($\overline{\text{BREQ}}$)
R00–R07/A0–A7	124–131	36–43	O	Output terminals (R00–R07) or address bus (A0–A7)
R10–R17/A8–A15	132–139	44–51	O	Output terminals (R10–R17) or address bus (A8–A15)
R20–R22/A16–A18	140–142	52–54	O	Output terminals (R20–R22) or address bus (A16–A18)
R23/$\overline{\text{RD}}$	143	55	O	Output terminal (R23) or read signal output terminal ($\overline{\text{RD}}$)
R24/$\overline{\text{WR}}$	144	56	O	Output terminal (R24) or write signal output terminal ($\overline{\text{WR}}$)
R25/CL	145	57	O	Output terminal (R25) or LCD synchronous signal output terminal (CL)
R26/FR/$\overline{\text{TOUT}}$*	146	58	O	Output terminal (R26) or LCD frame signal (FR) output terminal * $\overline{\text{TOUT}}$ output is available for using as the E0C888xx.
R27/TOUT	147	59	O	Output terminal (R27) or programmable timer underflow signal output terminal (TOUT)
R30–R33/$\overline{\text{CE0}}$–$\overline{\text{CE3}}$	148–151	60–63	O	Output terminals (R30–R33) or chip enable output terminals ($\overline{\text{CE0}}$–$\overline{\text{CE3}}$)
R34/FOUT	152	64	O	Output terminal (R34) or clock output terminal (FOUT)
R35–R37	153–155	65–67	O	Output terminals (R35–R37)
R50/BZ	157	69	O	Output terminal (R50) or buzzer output terminal (BZ)
R51/$\overline{\text{BACK}}$/$\overline{\text{BZ}}$*	158	70	O	Output terminal (R51) or bus acknowledge signal output terminal ($\overline{\text{BACK}}$) * $\overline{\text{BZ}}$ output is available for using as the E0C888xx.
P00–P07/D0–D7	123–116	35–28	I/O	I/O terminals (P00–P07) or data bus (D0–D7)
P10/SIN	111	23	I/O	I/O terminal (P10) or serial I/F data input terminal (SIN)
P11/SOUT	110	22	I/O	I/O terminal (P11) or serial I/F data output terminal (SOUT)
P12/$\overline{\text{SCLK}}$	109	21	I/O	I/O terminal (P12) or serial I/F clock I/O terminal ($\overline{\text{SCLK}}$)
P13/$\overline{\text{SRDY}}$	108	20	I/O	I/O terminal (P13) or serial I/F ready signal output terminal ($\overline{\text{SRDY}}$)
P14/CMPP0	107	19	I/O	I/O terminal (P14) ,comparator 0 non-inverted input terminal or A/D converter input terminal
P15/CMPM0	106	18	I/O	I/O terminal (P15) ,comparator 0 inverted input terminal or A/D converter input terminal
P16/CMPP1	105	17	I/O	I/O terminal (P16) ,comparator 1 non-inverted input terminal or A/D converter input terminal
P17/CMPM1	104	16	I/O	I/O terminal (P17) ,comparator 1 inverted input terminal or A/D converter input terminal
COM0–COM15	159–174	71–86	O	LCD common output terminals
COM16–COM31 /SEG66–SEG51	65–50	153–138	O	LCD common output terminals (when 1/32 duty is selected) or LCD segment output terminal (when 1/16 duty is selected)
SEG0–SEG50	175–176, 1–49	87–137	O	LCD segment output terminals
$\overline{\text{RESET}}$	92	4	I	Initial reset input terminal
$\overline{\text{TEST}}$	91	3	I	Test input terminal
AV_{DD}	112	24	–	Analog circuit system power supply (+) terminal
AV_{SS}	113	25	–	Analog circuit system power supply (–) terminal
AV_{REF}	114	26	–	Analog circuit system reference voltage terminal
TXD	72	160	O	Serial data output terminal for Flash programming
RXD	70	158	I	Serial data input terminal for Flash programming
SCLK	71	159	I/O	Serial clock I/O terminal for Flash programming
CLKW	68	156	I	Clock input terminal for Flash programming
XSPRG	67	155	I	Test input terminal for Flash programming
VEPEXT	69	157	–	Flash test terminal (High voltage circuit monitor terminal)

Notes:
- The pin assignment of the E0C88F360 (QFP18-176pin) is incompatible with the E0C883xx/E0C888xx.
- "*" indicates that the pin function of the E0C888xx differs from that of the E0C883xx.
- The Flash memory in the E0C88F360 can be programmed with a single power source (4.5 V to 5 V).

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